What is claimed is:

1. A wafer pattern shape evaluation device for evaluating a pattern shape formed on a semiconductor wafer in accordance with CAD data, comprising:

designating means for designating, using CAD data, a subject pattern to be evaluated;

means for acquiring CAD line segment data corresponding to SEM image data for the subject pattern and the subject pattern in response to the designating means;

means for performing line segment extraction for the subject pattern based on SEM image data in order to obtain SEM line segment data;

evaluation processing means for subjecting the subject pattern to two-dimensional evaluation processing based on the CAD line segment data and the SEM line segment data;

displaying means for displaying evaluation results from the evaluation processing means;

2. The semiconductor wafer pattern shape evaluation device of claim 1, wherein the CAD line segment data is made based on data corresponding to the subject pattern of the CAD data.

3. The semiconductor wafer pattern shape evaluation device of claim 1, wherein evaluation items occurring in two dimensional evaluation processing comprise at least one of pattern endpoints, width, interval and surface area.

4. The semiconductor wafer pattern shape evaluating device of claim 1, wherein the two-dimensional evaluation processing includes a process of calculating superimposition displacement distances between CAD line segment data and SEM line segment data for noted line segments of a subject pattern.

5. The semiconductor wafer pattern shape evaluation device of claim 1, wherein the superimposition displacement distance is compared with a prescribed reference value, with evaluation values corresponding to the superimposition displacement distances being taken as the display evaluation results.

6. The semiconductor wafer pattern shape evaluation device of claim 1, wherein the superimposition displacement distance is compared with a prescribed reference value, with evaluation values corresponding to the superimposition displacement distances being assigned levels and being taken as the display evaluation results.

7. The semiconductor wafer pattern shape evaluating device of claim 1, wherein the superimposition displacement distance is compared with a prescribed reference value, evaluation values corresponding to superimposition displacement distances are assigned levels, with the evaluation values being displayed at the display means using colors or patterns etc. predefined for each level.

8. The semiconductor wafer pattern shape evaluating device of claim 7, wherein evaluation values for each location of the subject pattern are displayed at corresponding locations on a wafer map.

9. A method for evaluating a pattern shape formed on a semiconductor wafer in accordance with CAD data, comprising the step of:
extracting line segments for a subject pattern based on SEM image data for the subject pattern to be evaluated and acquiring SEM line segment data, and evaluating the subject pattern in two dimensions based on CAD line segment data corresponding to the subject pattern and SEM line segment data.

10. The semiconductor wafer pattern shape evaluation method of claim 9, wherein the CAD line segment data is made based on data corresponding to the subject pattern of the CAD data.

11. The semiconductor wafer pattern shape evaluation method of claim 10, wherein evaluation items occurring in two-dimensional evaluation comprise at least one of pattern endpoints, width, interval and surface area.

12. The semiconductor wafer pattern shape evaluating method of claim 10, wherein the two-dimensional evaluation processing includes a process of calculating superimposition

displacement distances between CAD line segment data and SEM line segment data for noted line segments of a subject pattern.

13. The semiconductor wafer pattern shape evaluation method of claim 12, wherein the superimposition displacement distance is compared with a prescribed reference value, with evaluation values corresponding to the superimposition displacement distances being taken as the display evaluation results.

14. The semiconductor wafer pattern shape evaluation method of claim 12, wherein the superimposition displacement distance is compared with a prescribed reference value, with evaluation values corresponding to the superimposition displacement distances being assigned levels and being taken as the display evaluation results.

15. The semiconductor wafer pattern shape evaluating method of claim 1, wherein the superimposition displacement distance is compared with a prescribed reference value, evaluation values corresponding to superimposition displacement distances are assigned levels, with the evaluation values being displayed using colors or patterns etc. predefined for each level.

16. The semiconductor wafer pattern shape evaluating method of claim 9, wherein evaluation values for each location of the subject pattern are displayed at corresponding locations on a wafer map.